REMARKS

In response to the above-identified Office Action, Applicants amend the application and seek reconsideration thereof. In this response, Applicants amend Claims 21-27 and 29. No claims have been cancelled and no new claims have been added. Accordingly, Claims 20-29 are pending.

I. Specification

Applicants amend the Specification to provide the required reference to the prior Application. Accordingly, Applicants respectfully request withdrawal of the objection to the Specification.

Applicants amend claims 21-22, 24, 26-27, and 29 without adding new matter and not to overcome any rejection or prior art or for any reason related to a statutory requirement for patentability.

II. Claims Rejected Under 35 U.S.C. §112, Second Paragraph

The Examiner rejects Claims 23 and 25-29 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter, which Applicants regard as the invention.

Applicants amend Claims 23 and 25 to correct the lack of antecedent basis therein. Regarding Claim 27, the Examiner argues that the limitation "the doped regent" in lines 5-6 lacks an antecedent basis. Applicants note that on line 4 of Claim 27, however, the limitation "a doped region" provides the antecedent basis for "the doped region" in lines 5-6.

Accordingly, Applicants respectfully request withdrawal of the rejection of Claims 23, 25, and 27. Claim 26 depends from Claim 25. Claims 28-29 depend from Claim 27. As such, the rejected dependent claims are not indefinite for at least the same reasons as the claims from which they depend.

III. Claims Rejected Under 35 U.S.C. §102(e)

The Examiner rejects Claims 20-23 and 27-29 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,218,706 B1 to Waggoner et al. ("Waggoner"). Applicants respectfully traverse this rejection.

To anticipate a claim, every element of the claim must be disclosed within a single reference. Among other limitations, independent Claim 20 recites forming a performance circuit occupying a first area of an integrated circuit substrate and forming a protection circuit occupying a second area of an integrated circuit substrate separate from the first area.

In making the rejection, the Examiner relies on Waggoner to show a performance circuit (T_1, T_2) in combination with a protection circuit (D_3). (Waggoner, FIG. 8.) However, FIG. 8 and the accompanying text do not disclose a performance circuit and a protection circuit occupying separate substrate areas. (Waggoner, FIG. 8, col. 8, lines 23-40.) In contrast, Waggoner discloses that the performance circuit (T_1, T_2) and protection circuit (D_3) are integrated and, additionally, are connected to the same V_{DD} rail. See id. Thus, the cited text and accompanying figure to teach or suggest forming a performance circuit occupying a first area of an integrated circuit substrate and forming a protection circuit occupying a second area of an integrated circuit substrate separate from the first area.

Accordingly, Applicants respectfully request withdrawal of the rejection of independent Claim 20. Claims 21-23 and 27-29 depend from Claim 20. As such, the rejected dependent claims are not anticipated for at least the same reasons as their respective independent claim.

IV. Claims Rejected Under 35 U.S.C. §103(a)

The Examiner rejects Claims 24-26 under 36 U.S.C. §103(a) as being obvious over Waggoner in view of U.S. Patent No. 6,274,908 B1 to Yamaguchi et al. ("Yamaguchi"). Applicants respectfully traverse this rejection.

The Examiner's obligation in making a *prima facie* case of obviousness requires the Examiner to show that the prior art, in combination, teaches or suggests

all elements of the claimed invention. Applicants respectfully submit that the Examiner has failed to set forth a *prima facie* case of obviousness.

Claims 24-26 depend from Claim 20. Among other limitations, independent Claim 20 recites forming a performance circuit occupying a first area of an integrated circuit substrate and forming a protection circuit occupying a second area of an integrated circuit substrate separate from the first area.

As argued above, Waggoner fails to teach or suggest forming a performance circuit and a protection circuit that occupy separate substrate areas. The Examiner relies on Yamaguchi to show formation of a unit diode. (Yamaguchi, Figure 11.) However, Yamaguchi also does not disclose forming a performance circuit and a protection circuit wherein both occupy separate substrate areas. Rather, Yamaguchi discloses that a protection circuit maybe divided into electrically isolated islands. (Yamaguchi, col. 23, lines 1-20.) Since neither Waggoner nor Yamaguchi teach or suggest forming a performance circuit occupying a first area of an integrated circuit substrate and forming a protection circuit occupying a second area of an integrated circuit substrate separate from the first area, they cannot be combined to do so.

Accordingly, Applicants respectfully request the withdrawal of the rejection of Claims 24 and 25. Claim 26 depends from Claim 25. As such, Claim 26 is not obvious for at least the same reason as Claim 25.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending are now in condition for allowance and such action is earnestly solicited at the earliest possible date. If there are any fees due in connection with the filing of this response, please charge those fees to our Deposit Account No. 02-2666.

If any matters can be resolved by telephone, Applicants request that the Patent and Trademark Office call the Applicants' attorney at the telephone number listed below.

Respectfully submitted,

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CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited as First Class Mail with sufficient postage with the United States Postal Service in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on February 4, 2002.

Diane Martinez February 4, 2002

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

21. The method of claim 20, wherein ~~the step of~~ forming a performance circuit includes a forming a CMOS ~~device~~ configuration.

22. The method of claim 21, wherein ~~the step of~~ coupling the protection circuit to the performance circuit includes coupling the protection circuit to a p-channel device of the CMOS ~~device~~ configuration.

23. The method of claim 21, wherein ~~the step of~~ forming a protection circuit includes forming a diode and ~~the step of~~ coupling the protection circuit to the performance circuit includes coupling the diode to ~~the~~ a p-channel device of the CMOS configuration.

24. The method of claim 20, wherein ~~the step of~~ forming a protection circuit includes forming a unit diode, the unit diode comprised of a block of a doped region of the integrated circuit substrate occupying an area of the substrate sufficient to support a contact to the doped region, a junction region of the integrated circuit substrate surrounding the doped region, and a contact to the doped region.

25. The method of claim 20, ~~the~~ a doped region being a first doped region of a first dopant in a well of the substrate, the well being doped with a first concentration of a second dopant and ~~the~~ a junction region separating the first doped region from the well, wherein ~~the step of~~ forming a protection circuit includes forming a third

doped region in the well adjacent the junction region, the third doped region doped with a second concentration of the second dopant.

26. The method of claim 25, wherein ~~the step of~~ forming a protection circuit includes forming a plurality of unit diodes.

27. The method of claim 20, wherein ~~the step of~~ forming a performance circuit includes:

forming a unit transistor device having a drain region comprised of a doped region of the integrated circuit substrate occupying an area sufficient to support a contact to the doped region;

forming a gate region of the integrated circuit substrate surrounding the doped region; and

forming a contact to the doped region.

29. The method of claim 28, wherein ~~the step of~~ forming a performance circuit includes:

forming a plurality of unit transistors.